

Application No.: 10/767,623

Docket No.: JCLA8288-D

AMENDMENT

In The Claims:

Please amend the claims as follows:

Claims 1-5 (cancelled).

6. (currently amended) A process for forming a semiconductor packaging substrate, comprising:

forming a laminated circuit having a first surface and a second surface opposite to the first surface, wherein the laminated circuit has a plurality of patterned internal metal layers stacked up, and has a plurality of internal insulation layers each of which is interposed between two adjacent internal metal layers;

forming at least one contact via through the internal metal layers and the internal insulation layers, such that the internal metal layers electrically connect to one another;

forming a first external insulation layer and a second external insulation layer respectively on the first surface and the second surface of the laminated circuit, wherein the first external insulation layer has at least one first opening and the external second insulation layer has at least one second opening;

forming a first via in ~~each~~ of the first opening and a second via in ~~each~~ of the second opening;

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forming a first external metal layer on the first external insulation layer and a second external metal layer on the second external insulation layer, wherein the first and second external metal ~~layer~~ layers are electrically connected to the internal metal layers of the laminated circuit respectively through the first and second vias, and wherein the first external metal layer has a plurality of first externally exposed areas and the second external metal layer has a plurality of second externally exposed areas.

7. (original) The process of claim 6, wherein the forming the contact via includes mechanically drilling and plating on the laminated circuit.

8. (original) The process of claim 6, wherein the forming the first and the second vias includes non-mechanically drilling and plating on the first and second external insulation layers, respectively.

9. (original) The process of claim 7, wherein the non-mechanically drill is selected from a group consisting of photo-via forming, laser ablating and plasma etching.

10. (original) The process of claim 6, further comprising a step of forming a first solder mask on the first external metal layer to cover the first external insulation layer and expose the first externally exposed areas, after forming the first external metal layer.

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11. (original) The process of claim 6, further comprising a step of forming a second solder mask on the second external metal layer to cover the second external insulation layer and expose the second externally exposed areas, after forming the second external metal layer.

12. (original) The process of claim 6, wherein the semiconductor packaging substrate is a flip-chip ball grid array packaging substrate.

13. (original) The process of claim 6, wherein forming the internal metal layers of the laminated circuit includes forming and patterning copper foils.

Claims 14-17 (cancelled).

18. (new) A process for forming a semiconductor packaging substrate, comprising:
performing a lamination process for forming a laminated circuit including the steps of:
 providing at least two sheets, each sheet having a patterned conductive layer formed thereon;
 interposing a bonding sheet between the two sheets;
 performing a thermal compression process so that the bonding sheet adheres the two sheets; and

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forming at least one contact via through the two sheets and the bonding sheet such that the patterned conductive layers formed on the two sheets are electrically connected to each other; and

performing a build-up process comprising:

forming a first insulation layer and a second insulation layer respectively on a first surface and a second surface of the laminated circuit, wherein the first insulation layer comprises at least one first opening and the second insulation layer comprises at least one second opening;

forming a first via in the first opening and a second via in the second opening;

forming a first metal layer on the first insulation layer and a second metal layer on the second insulation layer, wherein the first metal layer and second metal layer are electrically connected to the patterned conductive layers of the laminated circuit respectively through the first and second vias.

19. (new) The process of claim 18, wherein the step of forming the contact via includes mechanically drilling and plating process.

20. (new) The process of claim 18, wherein the step of forming the first and the second vias includes performing non-mechanically drilling and plating process on the first and second external insulation layers, respectively.

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21. (new) The process of claim 19, wherein the step of non-mechanically drilling is selected from a group consisting of a photo-via process, laser ablating and a plasma etching process.

22. (new) The process of claim 18, further comprising a step of forming a first solder mask on the first external metal layer to cover the first external insulation layer and expose the first externally exposed areas, after forming the first external metal layer.

23. (new) The process of claim 18, further comprising a step of forming a second solder mask on the second external metal layer to cover the second external insulation layer and expose the second externally exposed areas, after forming the second external metal layer.

24. (new) The process of claim 18, wherein the semiconductor packaging substrate is a flip-chip ball grid array packaging substrate.

25. (new) The process of claim 18, wherein forming the internal metal layers of the laminated circuit includes forming and patterning copper foils.